In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. – 8. (Canceled)

9. (Original) A thin film transistor (TFT) structure, comprising:

a plurality of stacked structures on a substrate, said plurality of stacked structures including a first conducting layer, an insulation layer, an amorphous silicon layer and an ohmic contact layer;

a photo-imagable layer between said plurality of stacked structures;

a source electrode and a drain electrode on said photo-imagable layer, wherein said source electrode is connected to a portion of said amorphous silicon layer and said drain electrode is connected to another portion of said amorphous silicon layer;

a passivation layer on said amorphous silicon layer, said source electrode and said drain electrode; and

a transparent electrode on said passivation layer and electrically connected to one of said source electrode and said drain electrode.

10. (Original) The TFT structure according to claim 9, wherein said plurality of stacked structures are formed by one mask manufacturing.

11. (Original) The TFT structure according to claim 9, wherein said first conducting layer is a gate electrode.

12. (Original) The TFT structure according to claim 9, wherein each said source electrode and said drain electrode comprise a second conducting layer and an ohmic contact layer, said second conducting layer is positioned between said amorphous silicon layer and said passivation layer, said ohmic contact layer is positioned between said amorphous silicon layer and said second conducting layer, such that said second conducting layer connects to said amorphous silicon layer through said ohmic contact layer.

13. (Original) A thin film transistor (TFT) structure, comprising:

a plurality of first stacked structures and a plurality of second stacked structures on a substrate, wherein each first stacked structure includes a first conducting layer, an insulation layer, an amorphous silicon layer and an ohmic contact layer, and each second stacked structure at least includes said first conducting layer;

a photo-imagable layer between said plurality of first stacked structures and said plurality of said second stacked structures;

a source electrode and a drain electrode on said photo-imagable layer and said plurality of first stacked structures;

a passivation layer on said photo-imagable layer and said source electrode and said drain electrode; and

a transparent electrode on said passivation layer wherein a first portion of said transparent electrode electrically connects to one of said source electrode and drain electrode, and a second portion of said transparent electrode electrically connects said second conducting layer of said plurality of first stacked structures and said first conducting layer of said plurality of second stacked structure.

14. (Original) The TFT structure according to claim 13, wherein said plurality of first stacked structures and said plurality of second stacked structures are formed by one mask manufacturing.

15. (Original) The TFT structure according to claim 13, wherein each said source electrode and said drain electrode comprise a second conducting layer and an ohmic contact layer, said second conducting layer is positioned under said passivation layer, said ohmic contact layer is positioned between said amorphous silicon layer and said second conducting layer, such that said second conducting layer connects to said amorphous silicon layer of said plurality of first stacked structures through said ohmic contact layer.